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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/940,324	08/27/2001	Robert T. George	2207/12003	5090

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EXAMINER	
KIM, HONG CHONG	
ART UNIT	**PAPER NUMBER**
2185	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/940,324	GEORGE ET AL.	
	Examiner	Art Unit	
	Hong C. Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-17 are presented for examination. This office action is in response to the amendment filed on 3/8/07.

Information Disclosure Statement

2. Applicants are reminded of the duty to disclose information under 37 CFR 1.56.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Wilson US patent No. 6,560,681 or Barroso et al. (Barroso) US Patent No. 6,668,308.

As to claim 1, Wilson discloses a cache-coherent I/O device (Fig. 4) comprising: a plurality of client ports (connections between Refs. 412 & Ref. 422 and 414 & 424), each to be coupled to one of a plurality of port components (Fig. 4 Refs. 412 and 414); a plurality of sub-unit caches (Fig. 4 Refs. 422 and 424), each coupled to one of said plurality of client ports and assigned to one of said plurality of port components

(connections between Refs. 412 & Ref. 422 and 414 & 424); and a coherency engine (Fig. 4 Ref. 450) coupled to said plurality of sub-unit.

Alternatively, Barroso discloses a cache-coherent I/O device (Fig. 1) comprising: a plurality of client ports (connections between Refs. 110's & 121's), each to be coupled to one of a plurality of port components (Fig. 1 Refs. 110's); a plurality of sub-unit caches (Refs. 121's), each coupled to one of said plurality of client ports and assigned to one of said plurality of port components (col. 4 lines 17-18); and a coherency engine (Fig. 1 Ref. 140 & Fig. 4 and col. 11 lines 23-27 & col. 4 lines 18-19) coupled to said plurality of sub-unit.

As to claim 2, Wilson and Barroso disclose the invention as claimed in the above. Wilson further discloses wherein said plurality of port components includes processor port components (Fig. 4 Refs. 412 and 414). Barroso further discloses wherein said plurality of port components includes processor port components (Fig. 1 Refs. 110).

As to claim 3, Wilson and Barroso disclose the invention as claimed in the above. Wilson further discloses wherein said plurality of port components includes input/output components (Fig. 4 Refs. 412 and 414). Barroso further discloses wherein said plurality of port components includes input/output components (Fig. 1 Refs. 110).

As to claim 4, Wilson and Barroso disclose the invention as claimed in the above. Wilson further discloses wherein said plurality of sub-unit caches includes transaction

buffers (col. 3 line 38-40) using a coherency logic protocol (col. 3 lines 32-33). Barroso further discloses wherein said plurality of sub-unit caches includes transaction buffers (col. 8 line 15-16) using a coherency logic protocol (Fig. 4).

As to claim 5, Wilson and Barroso disclose the invention as claimed in the above. Barroso further discloses the coherency logic protocol includes a Modified-Exclusive-Shared-Invalid (MESI) cache coherency protocol (col. 8 lines 16-18).

As to claim 6, Wilson discloses a processing system comprising (Fig. 4): a processor (Fig. 4 Ref 402); a plurality of port components (Fig. 4 Refs. 412 and 414); and a cache-coherent I/O device (Fig. 4 Ref 410) coupled to said processor and including a plurality of client ports (connections between Refs. 412 & Ref. 422 and 414 & 424), each coupled to one of said plurality of port components, said cache-coherent device further including a plurality of caches (Fig. 4 Refs. 422 and 424), each coupled to one of said plurality of client ports and assigned to one of said plurality of port components (connections between Refs. 412 & Ref. 422 and 414 & 424), and a coherency engine (Fig. 4 ref. 450) coupled to said plurality of caches.

Alternatively, Barroso discloses a processing system comprising (Fig. 3): a processor (Fig. 3 Ref 10); a plurality of port components (Fig. 1 Refs. 110's); and a cache-coherent I/O device (Fig. 1) coupled to said processor and including a plurality of client ports (connections between Refs. 110's & 121's), each coupled to one of said plurality of port components, said cache-coherent device further including a plurality of

caches (Fig. 1 Refs. 121's), each coupled to one of said plurality of client ports and assigned to one of said plurality of port components (col. 4 lines 17-18), and a coherency engine (Fig. 1 Ref. 140 & Fig. 4 and col. 11 lines 23-27 7 col. 4 lines 18-19) coupled to said plurality of caches.

As to claim 7, Wilson and Barroso disclose the invention as claimed in the above. Wilson further discloses wherein said plurality of port components includes processor port components (Fig. 4 Refs. 412 and 414). Barroso further discloses wherein said plurality of port components includes processor port components (Fig. 1 Refs. 110).

As to claim 8, Wilson and Barroso disclose the invention as claimed in the above. Wilson further discloses wherein said plurality of port components includes input/output components (Fig. 4 Refs. 412 and 414). Barroso further discloses wherein said plurality of port components includes input/output components (Fig. 1 Refs. 110).

As to claim 9, Wilson discloses the invention as claimed. Wilson discloses a method comprises receiving a transaction request (Fig, 5 Ref. 502) at one of said plurality of client ports (connections between Refs. 412 & Ref. 422 and 414 & 424) on the I/O cache-coherent device (Fig. 4), said transaction request includes an address (Fig. 5 ref. 512, address); and determining whether said address is present (Fig. 5 ref. 512, compare) in a plurality of sub unit-caches (Fig. 4 Refs. 422 and 424), each of said

sub-unit caches assigned to said one of said plurality of client ports (connections between Refs. 412 & Ref. 422 and 414 & 424).

Alternatively, Barroso discloses a method comprises receiving a transaction request (col. 7 lines 62-64, executing instruction set) at one of said plurality of client ports (connections between Fig. 1 Refs. 110's & 121's) on the I/O cache-coherent device (Fig. 1), said transaction request includes an address (col. 8 line 12, tag compare); and determining whether said address is present (col. 8 line 12, tag compare) in a plurality of sub unit-caches (Ref. 121's), each of said sub-unit caches assigned to said one of said plurality of client ports (col. 4 lines 17-18).

As to claim 10, Wilson and Barroso disclose the invention as claimed in the above. Wilson further discloses wherein said transaction request is a read transaction request (Fig. 5 Ref. 502, col. 5 lines 37-42). Barroso further discloses wherein said transaction request is a read transaction request (col. 7 lines 62-64, executing instruction set).

As to claim 11, Wilson and Barroso disclose the invention as claimed in the above. Wilson further discloses transmitting data for said read transaction request from said one of said plurality of sub-unit caches to one of said plurality of client ports (Fig. 5 Ref. 528). Barroso further discloses transmitting data for said read transaction request from said one of said plurality of sub-unit caches to one of said plurality of client

ports (col. 8 lines 12, tag compare logic reads on this limitation since tag compare operation including read and write operations).

As to claim 12, Wilson and Barroso disclose the invention as claimed in the above. Wilson further discloses prefetching one or more cache lines ahead of said read transaction request (cache memory reads on this limitation since the cache memory is used to assure that the currently useful data of main memory are copied into the small and fast cache for the purpose of increasing data access speed by means of spatial and temporal localities); and updating the coherency state (col. 3) information in said plurality of sub-unit caches. Barroso further discloses prefetching one or more cache lines ahead of said read transaction request (cache memory reads on this limitation since the cache memory is used to assure that the currently useful data of main memory are copied into the small and fast cache for the purpose of increasing data access speed by means of spatial and temporal localities); and updating the coherency state (col. 8 lines 15-20) information in said plurality of sub-unit caches.

As to claim 13, Wilson and Barroso disclose the invention as claimed in the above. Barroso further discloses the coherency logic protocol includes a Modified-Exclusive-Shared-Invalid (MESI) cache coherency protocol (col. 8 lines 16-18).

As to claim 14, Wilson and Barroso disclose the invention as claimed in the above. Wilson further discloses wherein said transaction request is a write transaction

request (col. 5 lines 38-39). Barroso further discloses wherein said transaction request is a write transaction request (col. 7 lines 62-64, executing instruction set).

As to claim 15, Wilson and Barroso disclose the invention as claimed in the above. Barroso further discloses modifying coherency state information for a cache line in said one of said plurality of sub-unit caches; updating coherency state information in others of said plurality of sub-unit caches by said coherency engine; and transmitting data for said write transaction request from said one of said plurality of sub-unit caches to memory (MESI protocol reads on this limitation and col. 8 lines 16-20).

As to claim 16, Wilson and Barroso disclose the invention as claimed in the above. Barroso further discloses write transaction request in the order received and pipelining multiple write requests (col. 4 lines 44-46)

As to claim 17, Wilson and Barroso disclose the invention as claimed in the above. Barroso further discloses wherein the coherency state information includes a Modified-Exclusive-Shared-Invalid (MESI) cache coherency protocol (col. 8 lines 15-18).

4. Claims 5, 13, and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilson US patent No. 6,560,681 in view of Jim Handy, "The Cache Memory Handbook" TK7895.M4H35, 1993, pp 140-240.

As to claims 5 and 13, Wilson discloses the invention as claimed above. Although Wilson discloses a cache coherency protocol (col. 3), however, Wilson does not specifically disclose wherein said coherency logic protocol includes a Modified-Exclusive-Shared-Invalid (MESI) cache coherency protocol.

However, it is well known in the cache art to using MESI cache coherency protocol for the purpose of maintaining data consistency thereby increasing the memory access speed. For example, Handy discloses many different coherency logic protocols includes a Modified-Exclusive-Shared-Invalid (MESI) cache coherency protocol (Page 159).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to add the coherency logic protocol includes a Modified-Exclusive-Shared-Invalid (MESI) cache coherency protocol of Handy into the invention of Wilson for the advantages stated above.

As to claim 15, Wilson and Handy disclose the invention as claimed in the above. Handy further discloses modifying coherency state information for a cache line in said one of said plurality of sub-unit caches; updating coherency state information in others of said plurality of sub-unit caches by said coherency engine; and transmitting data for said write transaction request from said one of said plurality of sub-unit caches to memory (MESI protocol reads on this limitation and pages 159-161).

As to claim 16, Wilson and Handy disclose the invention as claimed in the above. Wilson further discloses write transaction request in the order received and pipelining multiple write requests (col. 5 line 41)

As to claim 17, Wilson and Handy disclose the invention as claimed in the above. Handy further discloses wherein the coherency state information includes a Modified-Exclusive-Shared-Invalid (MESI) cache coherency protocol (Page 159).

Response to Arguments

5. Applicant's arguments with respect to claims 1-17 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See attached PTO-892.

2. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

3. When responding to the office action, Applicant is advised to clearly point out the

patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. ' 1.111(c).

4. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hong C Kim whose telephone number is (571) 272-4181. The examiner can normally be reached on M-F 9:00 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 whose telephone number is (571) 272-2100.

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

7. **Any response to this action should be mailed to:**

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to TC-2100:
(571)-273-8300

Hand-delivered responses should be brought to the Customer Service Window (Randolph Building, 401 Dulany Street, Alexandria, VA 22314).

HK
Primary Patent Examiner
May 12, 2007